REMARKS

Summary of Office Action

Claims 1-37 are pending in the above-identified patent application.

The Examiner has rejected claims 1, 6, 24 and 25 under 35 U.S.C. 103(a) as allegedly being obvious from Kyles et al. U.S. Patent 6,008,680. Claim 11 has been rejected under 35 U.S.C. 103(a) as allegedly being obvious from Kyles in view of Li et al. U.S. Patent 6,693,985. Claims 12-15 have been rejected under 35 U.S.C. 103(a) as allegedly being obvious from Kyles and Li, further in view of Wang et al. U.S. Patent 6,292,116.

Each of claims 2-10, 17-23 and 26-37 has been objected to as depending from a rejected base claim, but allowable subject matter has been indicated.

Summary of Applicants' Reply

Applicants note with appreciation the indication of allowable subject matter in claims 2-10, 17-23 and 26-37, and hereby expressly reserve the right to rewrite any one or more of claims 2-10, 17-23 and 26-37 in independent form should its respective base claim ultimately not be allowed.

Applicants have amended the specification and claims 24 and 36 to correct typographical errors. The error in claim 36 was inadvertently introduced in the December 8, 2005 Reply to Office Action.

The Examiner's rejections are respectfully traversed.

Applicants' Reply

Claims 1, 6, 24 and 25 have been rejected under 35 U.S.C. 103(a) as allegedly being obvious from Kyles. Claim 11 has been rejected under 35 U.S.C. 103(a) as allegedly being obvious from Kyles in view of Li. Claims 12-15 have

been rejected under 35 U.S.C. 103(a) as allegedly being obvious from Kyles and Li, further in view of Wang. These rejections are respectfully traversed.

As previously noted, applicants' invention, as defined by independent claims 1 and 16, is directed to circuitry and a method for extracting data from a data signal having a data rate that is twice the frequency of a reference clock signal. A first phase-shifted version of the reference clock signal is derived that is synchronized with a rising edge (i.e., a 0-to-1 level transition) of the data signal. The data signal is sampled in a predetermined phase relationship to this first phase-shifted version to extract a first partial stream of data. A second phase-shifted version of the reference clock signal is also derived that is synchronized with a falling edge (i.e., a 1-to-0 level transition) of the data signal. The data signal is further sampled in a predetermined phase relationship to this second phase-shifted version to extract a second partial stream of data. Claims 1 and 16 define first and second versions of the reference clock signal "that are respectively synchronized with oppositely polarized transitions in level of the data signal."

Applicants' invention, as defined by independent claim 25, is directed to an apparatus for receiving an information signal. Claim 25 similarly recites that the recovered clock signals are "respectively synchronized with oppositely polarized transitions in level of the information signal."

Contrary to the Examiner's contentions, applicants respectfully submit that Kyles does not show or suggest deriving first and second versions of the reference clock signal "that are respectively synchronized with oppositely polarized transitions in level of the [data or information]

signal" as recited in applicants' independent claims 1, 16 and 25.

Kyles describes a continuously adjustable delay circuit for a delay-locked loop. Two delay paths receive a reference signal and provide delayed signals by delaying the reference signal in complementary manners in response to a tuning signal. The tuning signal is a filtered error signal based on a phase comparison between a received data signal and a recovered clock signal. The tuning signal thus is not the claimed "data signal." Moreover, to the extent that the tuning signal is related at all to the data signal, it represents phase delay between the clock signal and the data signal, not transitions in the data signal. Therefore Kyles does not provide any reference clock signals synchronized with transitions (of any polarity) in the level of the data signal.

For at least the foregoing reasons, applicants respectfully submit that independent claims 1, 16 and 25 are patentable. Each of claims 11-15 depends, directly or indirectly, from independent claim 1, and therefore each is patentable as well. Similarly, each of allowable but objected-to claims 2-10, 17-23 and 26-37 depends directly or indirectly from one of claims 1, 16 and 25, and is patentable in current form for that reason.

Conclusion

In view of the foregoing, applicants respectfully submit that this application, including claims 1-37, as

amended, is in condition for allowance. Reconsideration and allowance of this application are respectfully requested.

Respectfully submitted,

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